What is claimed is:

1. A process for cleaning copper surfaces of copper objects, without etching bulk copper from said objects, comprising contacting said surfaces with an aqueous solution comprising an inorganic acid, a persulfate salt and a phosphate salt.

2. The process as recited in claim 1, wherein said objects are copper features on intermediary and final structures of a microelectronic package, said microelectronic package comprising a dielectric substrate having at least one lateral outermost surface to which said copper features are attached.

3. The process as recited in claim 1, wherein said phosphate salt is selected from the group consisting of orthophosphate, metaphosphate, hydrogenphosphate and dihydrogenphosphate salts.

~~4. The process as recited in claim 3, wherein the cation in said phosphate salt is selected from the group consisting of ammonium, potassium, sodium, lithium, and water soluble alkaline metal cations.~~

5. The process as recited in claim 1, wherein said inorganic acid is selected from the group consisting of sulfuric acid, phosphoric acid, metaphosphoric acid and pyrophosphoric acid.

6. The process as recited in claim 1, wherein the cation in said persulfate salt is selected from the group consisting of alkali metals, ammonium and water soluble alkaline metal cations.

7. The process as recited in claim 1, wherein said aqueous solution comprises approximately 25-100 gm/liter sodium persulfate, up to about 3 volume% phosphoric acid, and up to about 0.116 Molar sodium phosphate.

8. The process as recited in claim 1, wherein said aqueous solution further comprises a surfactant.

9. The process as recited in claim 8, wherein said surfactant is anionic.

10. The process as recited in claim 9, wherein said anionic surfactant is selected from the group of compounds consisting of aryl sulfonates, alkyl sulfonates, aryl sulfates, alkyl sulfates and phosphate esters.

11. The process as recited in claim 8, wherein said surfactant is nonionic.

12. The process as recited in claim 11, wherein said nonionic surfactant is selected from the group of compounds consisting of nonyl phenol ethoxylated with 3-30 moles of ethylene oxide, octyl phenol ethoxylated with 3-30 moles of ethylene oxide, block copolymers of ethylene oxide and propylene oxide, and alkyl polyoxyalkylene ethers.

13. The process as recited in claim 2, wherein said copper features, comprise at least one of the group consisting of plated through holes, contact fingers, tabs, connecting pads, and external and fine line circuitry.

14. The process as recited in claim 13, wherein said intermediary and final structures of said microelectronic package further comprise precious metal/nickel or phosphorous/nickel plated features, wherein said surfaces of unplated said copper features are proximate said precious metal/nickel or phosphorous/nickel plated features, wherein said copper surfaces are unaffected by galvanic or accelerated etching of bulk copper from said aqueous solution.

15. The process as recited in claim 14, wherein said precious metal is gold or palladium.

16. The process as recited in claim 2, wherein said intermediary and final structures of said microelectronic package comprise an embedded nickel resistor.

17. A process to manufacture an intermediate structure of an embedded resistor printed wiring board, comprising the steps of:

a) providing a printed wiring board internal core comprising, a dielectric substrate having at least one_outermost lateral surface, copper features, and at least one nickel or nickel alloy planar resistor formed on said at least one of said outermost lateral surfaces; and

b) applying a microetch solution comprising an inorganic acid, a persulfate salt and a phosphate salt, to clean exposed surfaces of said copper features, without adversely affecting the resistor values of said at least one nickel or nickel alloy planar resistor.

18. The process to manufacture an embedded resistor printed wiring board, as described in claim 17, wherein said first and second dielectric substrates are selected from the group consisting of epoxy resins, polyimides, polytetrafluoroethylene (TEFLON), cyanates, cyanate esters, BT epoxies, and IBM Driclad epoxy, either unreinforced or reinforced with glass.

19. A process to manufacture a planar resistor in an intermediate structure printed wiring board, comprising the steps of:

a) providing a printed wiring board internal core comprising a dielectric substrate having at least one lateral outer surface and first copper features affixed to said at least one of said lateral outer surfaces;

b) applying a microetch solution comprising an inorganic acid, a persulfate salt and a phosphate salt, to said first copper features in order to clean exposed surfaces of said first copper features;

c) enhancing bond strength to subsequently applied dielectric materials by forming copper oxide on uppermost and sidewall surfaces of said first copper features;

d) applying a dielectric material to the first dielectric substrate to exposed said lateral outer surfaces of said dielectric substrate and to said first copper features in order to generate a multilayer laminate;

e) fabricating and plating through-holes through said dielectric material;

f) forming second copper features and at least one planar nickel or nickel alloy resistor on an uppermost surface of said dielectric material, said second copper features and said planar resistor being electrically connected to said first copper features through said plated through-holes; and

g) applying a microetch solution comprising an inorganic acid, a persulfate salt and a phosphate salt to said second copper features in order to clean exposed_ surfaces of said second copper features without adversely affecting the resistor values of said at least one nickel or planar nickel alloy resistor.

20. A process of manufacturing intermediary structures of a microelectronic package, comprising the steps of:

a) providing a microelectronic package comprising a dielectric substrate, said dielectric substrate having an outermost lateral surface with at least one component selected from the group consisting of unplated copper features, precious metal plated copper features, and copper circuit lines attached thereto;

b) applying an aqueous microetchant solution comprising inorganic acid, persulfate salt and phosphate salt, to said_microelectronic package in order to clean said unplated copper features, without causing galvanic etching of bulk copper from said components;

c) applying and processing a soldermask material to uppermost surfaces of said components in order to expose said copper features, while protecting said copper circuit lines with unprocessed soldermask material;

d) reapplying said aqueous microetchant solution from step (b), to said copper features in order to clean in-process oxides and other contaminants without galvanic etching of bulk copper from said copper features; and

e) applying an organic solderability preservative to said exposed unplated copper features to fabricate sites for mounting pads.